WHAT IS CLAIMED IS:

1. An early evaluation, self-timed phased logic gate, comprising:

a block compute function;

a master arrival detection function;

a trigger compute function;

a trigger arrival detection function;

a plurality of inputs; and

at least one block output;

wherein said at least one block output is capable of being updated by said block compute function upon the arrival of only a subset of said plurality of inputs as indicated by said trigger arrival detection function and said trigger compute function evaluating to true; and

wherein said at least one block output is capable of being updated by said block compute function upon the arrival of all of said plurality of inputs as indicated by said master arrival detection function and said trigger arrival detection function, and upon said trigger compute function evaluating to false.

2. The early evaluation, self-timed phased logic gate of Claim 1, further comprising:

a feedback output, wherein said feedback output is capable of being updated upon the arrival of all of said plurality of inputs as indicated by said master arrival detection function and said trigger arrival detection function.

3. The early evaluation, self-timed phased logic gate of Claim 1, wherein bundled signaling is utilized and said at least one block output is an output bundle.

4. The early evaluation, self-timed phased logic system of Claim 3, wherein said output bundle comprises at least one data wire and a phase signal.

5. The early evaluation, self-timed phased logic system of Claim 4, wherein said phase signal is inverted.

6. The early evaluation, self-timed phased logic system of Claim 4, wherein said phase signal is non-inverted.

7. The early evaluation, self-timed phased logic gate of Claim 1, wherein Level Encoded Dual Rail (LEDR) signaling is utilized and said at least one block output is a LEDR output comprising a value signal wire and a timing signal wire.

8. The early evaluation, self-timed phased logic system of Claim 7, wherein said LEDR output timing signal wire is inverted.

9. The early evaluation, self-timed phased logic system of Claim 7, wherein said LEDR output timing signal wire is non-inverted.

10. The early evaluation, self-timed phased logic gate of Claim 1, wherein said plurality of inputs includes at least one of the following signals: a master input; a trigger input; and a feedback input.

11. The early evaluation, self-timed phased logic gate of Claim 1, wherein said at least one block output is one of the following signals: a feedback output; and a current block output.

12. The early evaluation, self-timed phased logic gate of Claim 1, wherein said trigger arrival detection function produces a trigger phase signal upon detecting the arrival of a trigger input signal and a feedback input signal from among said plurality of inputs.

13. The early evaluation, self-timed phased logic gate of Claim 12, wherein said master arrival detection function produces a master phase signal upon detecting the arrival of a master input signal and said trigger phase signal.

14. The early evaluation, self-timed phased logic gate of Claim 13, wherein said block compute function produces said at least one block output from said master input signal.

15. The early evaluation, self-timed phased logic gate of Claim 13, wherein said block compute function produces said at least one block output from said master input signal and said trigger input signal.

16. The early evaluation, self-timed phased logic gate of Claim 13, wherein:

said trigger compute function computes the value of a phase select signal;

said phase select signal is used by a phase select multiplexer to select the value of a phase signal from either said master phase signal or said trigger phase signal; and

said phase signal causes said block compute function to update the value of said at least one block output.

17. A method for constructing an early evaluation, self-timed phased logic gate having a set of inputs and at least one current block output, said method comprising the steps of:

selecting a subset of the set of inputs for which early evaluation can be performed as trigger inputs, wherein the remainder of the set of inputs are master inputs;

constructing a first circuitry set that implements a first boolean function based upon the value of said trigger inputs, wherein the output of said first circuitry set is a phase select;

constructing a second circuitry set capable of detecting the arrival of said trigger inputs, wherein the output of said second circuitry set is a trigger phase;

constructing a third circuitry set that implements a second boolean function based upon the value of at least said master inputs, wherein the output of said third circuitry set is at least one new block output;

constructing a fourth circuitry set capable of detecting the arrival of said master inputs and said trigger phase, wherein the output of said fourth circuitry set is a master phase;

constructing a fifth circuitry set capable of selecting said trigger phase when said phase select is a first value, and capable of selecting said master phase when said phase select is a second value, wherein the output of said fifth circuitry set is a gate phase; and

constructing a sixth circuitry set capable of detecting the arrival of said gate phase and latching said gate phase and said at least one new block output, wherein the output of said sixth circuitry set is the at least one current block output.

18. The method of Claim 17, further comprising the step of:

updating said at least one new block output by said third set of circuitry upon the arrival of only said trigger inputs as indicated by said second set of circuitry and said phase select being equal to said first value.

19. The method of Claim 17, further comprising the step of:

updating said at least one new block output by said third set of circuitry upon the arrival of all inputs within the set of inputs, as indicated by said second and sixth sets of circuitry, and upon said phase select being equal to said second value.

20. The method of Claim 17, wherein bundled signaling is utilized and the at least one current block output is an output bundle.

21. The method of Claim 17, wherein Level Encoded Dual Rail (LEDR) signaling is utilized and the at least one current block output is a LEDR output comprising a value signal wire and a timing signal wire.